REMARKS

In the Office Action, the Examiner rejected claims 1-15 under § 102 as being anticipated

by USP 5,578,840 issued to Scepanovic et al (Scepanovic) and USP 5,822,214 issued to

Rostoker et al. (Rostoker). In this Amendment, Applicants have amended claims 1, 11, and 12. In

addition, Applicants have added claims 16-19. Accordingly, claims 1-19 will be pending after

entry of this Amendment.

I. Claims 1-11

The Examiner rejected claims 1-11 under § 102 as being anticipated by Scepanovic and

Rostoker.

Claims 2-11 are dependent directly or indirectly on independent claim 1. Claim 1 recites

an integrated-circuit ("IC") layout. This IC layout has several interconnect lines. The IC layout

further has a first set of Steiner points that are in the shape of a non-quadrilateral polygon, where

at least two interconnect lines intersect at each Steiner point.

Applicants respectfully submit that the cited references do not disclose teach, or even

suggest such an IC layout. Specifically, Applicants respectfully submit that the cited references

do not disclose an IC layout that has a first set of Steiner points that are in the shape of a non-

quadrilateral polygon. To add further force and reasoning to this argument, Applicants have

amended claim 1 to recite that at least two interconnect lines intersect at each Steiner point. (See

claim 1; see also, Figures 68 and 69).

The Examiner identified column 7, lines 39-42 of Scepanovic as disclosing the elements

of claim 1. However, this passage of Scepanovic discloses circuit cells having various shapes, not

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Steiner points. Therefore, Applicants respectfully submit that Scepanovic does not disclose, teach or even suggest the recited IC layout of claim 1 with it's non-quadrilateral Steiner points.

The Examiner identified column 18, lines 22-29 and column 86, lines 48-58 of Rostoker as disclosing the elements of claim 1. However, these passages of Rostoker disclose circuit cells and vias having various shapes, not Steiner points. Therefore, Applicants respectfully submit that Rostoker does not disclose, teach or even suggest the recited IC layout of claim 1 with its non-quadrilateral Steiner points.

As claims 2-11 are dependent on claim 1, Applicants respectfully submit that claims 2-11 are patentable over the cited references for at least the same reasons. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 102 rejection of claims 1-11.

II. Claims 12-15

The Examiner rejected claims 12-15 under § 102 as being anticipated by Scepanovic and Rostoker.

Claims 13-15 are dependent directly or indirectly on independent claim 12. Claim 12 recites an integrated-circuit ("IC") layout. This IC layout has several interconnect lines. The IC layout further has a first set of Steiner points, where each Steiner point in the first set has a circular shape, where at least two interconnect lines intersect at each Steiner point.

Applicants respectfully submit that the cited references do not disclose teach, or even suggest such an IC layout. Specifically, Applicants respectfully submit that the cited references do not disclose an IC layout that has first set of Steiner points, where each Steiner point in the first set has a circular shape. To add further force and reasoning to this argument, Applicants

Attny Docket: SPLX.P0106 PTO Serial Number: 10/066,102 have amended claim 12 to recite at least two interconnect lines intersect at each Steiner point.

(See claim 12; see also, Figures 68 and 69).

The Examiner identified column 7, lines 39-42 and column 8, lines 30-36 of Scepanovic

as disclosing the elements of claim 12. However, these passages of Scepanovic disclose circuit

cells having various shapes, not Steiner points. Furthermore Scepanovic, at a high-level,

discloses interconnect lines intersecting at general points, without specifying the shape of such

points. Therefore, Applicants respectfully submit that Scepanovic does not disclose, teach or

even suggest the recited IC layout of claim 12 with it's circular Steiner points.

The Examiner identified column 18, lines 22-29 and column 86, lines 48-58 of Rostoker

as disclosing the elements of claim 1. However, these passages of Rostoker disclose circuit cells

and vias having various shapes, not Steiner points. Furthermore Rostoker, at a high-level,

discloses interconnect lines intersecting at general points, without specifying the shape of such

points. Therefore, Applicants respectfully submit that Rostoker does not disclose, teach or even

suggest the recited IC layout of claim 12 with its circular Steiner points.

As claims 13-15 are dependent on claim 12, Applicants respectfully submit that claims

13-15 are patentable over the cited references for at least the same reasons. Furthermore,

Applicants respectfully submit that claims 13-15 recite many other patentable limitations. For

instance, Claim 14 recites interconnect lines having ends that are partially circular. In view of the

foregoing, Applicants respectfully request reconsideration and withdrawal of the § 102 rejection

of claims 12-15.

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III. New Claims 16-19

New independent claim 16 recites an integrated-circuit ("IC") layout. This IC layout has

several interconnect lines, where the interconnect-lines have ends that are partial non-

quadrilateral polygons. The IC layout further has several Steiner points that are in the shape of a

non-quadrilateral polygon, where at least two interconnect lines intersect at each Steiner point.

Applicants respectfully submit that the cited references do not disclose, teach, or even

suggest the IC layout recited in claim 16, as the cited references do not recite a IC layout that has

several interconnect lines, where the interconnect-lines have ends that are partial non-

quadrilateral polygons, and further has several Steiner points that are in the shape of a non-

quadrilateral polygon, where at least two interconnect lines intersect at each Steiner point. As

claims 17-19 are dependent on claim 16, Applicants respectfully submit that claims 17-20 are

patentable over the cited references for at least the same reasons as claim 16. Accordingly,

Applicants respectfully submit that claims 16-19 are patentable over the cited references.

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CONCLUSION

In view of the foregoing, it is submitted that all pending claims, namely claims 1-20, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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